IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

1. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first plurality of circuits for selectively providing a ~~first signal~~ path between ~~the second node end~~ the first node and a power supply signal node, each circuit in the first plurality of circuits comprising a first transistor and a second transistor, the first transistor having a control terminal coupled to the second node and the first transistor being coupled between the power supply signal node and the second transistor, the second transistor having a control terminal for receiving a control signal provided to said circuit and the second transistor being coupled between the first transistor and the first node, wherein each of said circuits ~~receives a~~ is controlled by the control signal so that only one of the first plurality of circuits provides the ~~second signal~~ path between the first node and the power supply signal node at any one time;

a second plurality of circuits for selectively providing a ~~second signal~~ path between ~~the second node and~~ the third node and a reference node, each circuit in the second plurality of circuits comprising a first transistor and a second transistor, the first transistor having a control terminal coupled to the second node and the first transistor being coupled between the reference node and the second transistor, the second transistor having a control terminal for receiving a control signal provided to said circuit and the second transistor being coupled between the first transistor and the third node, wherein each of said circuits ~~receives a~~ is controlled by the control signal so that only one of the second plurality of circuits provides the ~~second signal~~ path between the third node and the reference node at any one time.

2. Cancelled.

3. (Amended) The circuit of claim 1 ~~2~~ wherein:

the transistors in each circuit in the first plurality of circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the first plurality of circuits; and

the transistors in each circuit in the second plurality of circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the second plurality of circuits.

4. (Amended) The circuit of claim 1 ~~2~~ wherein:

the first transistor, the second transistor, and the transistors in each circuit in the first plurality of circuits are of a first type; and

the third transistor, the fourth transistor, and the transistors in each circuit in the second plurality of circuits are of a second type.

5. (Original) The circuit of claim 4 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

6. (Original) The circuit of claim 5 wherein:

the first transistor in each circuit in the first plurality of circuits has a different threshold voltage magnitude from that of the first transistor in any other circuit in the first plurality of circuits; and

the first transistor in each circuit in the second plurality of circuits has a different threshold voltage magnitude from that of the first transistor in any other circuit in the second plurality of circuits.

7. (Original) The circuit of claim 4 wherein

a source terminal of the first transistor is coupled to the reference node and a drain terminal of the first transistor is coupled to the first node;

a source terminal of the second transistor is coupled to the first node and a drain terminal of the second transistor is coupled to the second node;

a drain terminal of the third transistor is coupled to the second node and a source terminal of the third transistor is coupled to the third node;

a drain terminal of the fourth transistor is coupled to the third node and a source terminal of the fourth transistor is coupled to the power supply signal node;

in each circuit in the first plurality of circuits, a drain terminal of the first transistor is coupled to the power supply signal node, a source terminal of the first transistor is coupled to a drain terminal of the second transistor, and a source terminal of the second transistor is coupled to the first node; and

in each circuit in the second plurality of circuits, a drain terminal of the first transistor is coupled to the reference node, a source terminal of the first transistor is coupled to a drain terminal of the second transistor, and a source terminal of the second transistor is coupled to the third node.

8. (Original) The circuit of claim 1 wherein the first and second plurality of circuits each consists of first and second circuits, wherein the first circuits in each plurality of circuits receive a common control signal and the second circuits in each plurality of circuits receive a complementary version of said common control signal.

9. (Original) The circuit of claim 1 wherein the control signals provided to each circuit are programmable settings.

10. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a plurality of first circuits for selectively providing a ~~first signal~~ path between ~~the second node and~~ the first node and a power supply signal node, each first circuit comprising a first transistor and a second transistor, the first transistor having a control terminal coupled to the second node and the first transistor being coupled between the power supply signal node and the second transistor, the second transistor having a control terminal for receiving a control signal provided to said circuit and the second transistor being coupled between the first transistor and the first node, wherein each of the first circuits ~~receives a~~ is controlled by the control signal so that only one of the first circuits provides the ~~first signal~~ path at any one time; and a second

circuit for providing a ~~second signal~~ path between ~~the second node and~~ the third node and a reference node, the second circuit comprising a transistor having a control terminal coupled to the second node and said transistor being coupled between the reference node and the third node.

11. Cancelled

12. (Amended) The circuit of claim 10 ~~11~~ wherein:

the transistors in each of the plurality of first circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other first circuit.

13. (Amended) The circuit of claim 10 ~~11~~ wherein:

the first transistor, the second transistor, and the transistors in each of the plurality of first circuits are of a first type; and

the third transistor, the fourth transistor, and the transistor in the second circuit are of a second type.

14. (Original) The circuit of claim 13 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

15. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first circuit for providing a ~~first signal~~ path between ~~the second node end and~~ the first node and a power supply node, the first circuit comprising a transistor having a control terminal coupled to the second node and the transistor being coupled between the power supply node and the first node; and

a plurality of second circuits for selectively providing a ~~second signal~~ path between ~~the second node and~~ the third node and a reference node, each circuit in the plurality of second circuits comprising a first transistor and a second transistor, the first transistor having a control

terminal coupled to the second node and the first transistor being coupled between the reference node and the second transistor, the second transistor having a control terminal for receiving a control signal provided to said circuit and the second transistor being coupled between the first transistor and the third node, wherein each of the second circuits ~~receives a~~ is controlled by the control signal so that only one of the second circuits provides the ~~second signal~~ path between the third node binds the reference node at any one time.

16. Cancelled

17. (Amended) The circuit of claim 15 ~~16~~ wherein:

the transistors in each of the plurality of second circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other second circuit.

18. (Amended) The circuit of claim 15 ~~16~~ wherein:

the first transistor, the second transistor, and the transistor in the first circuit are of a first type; and

the third transistor, the fourth transistor, and the transistors in each of the plurality of second circuits are of a second type.

19. (Original) The circuit of claim 18 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

20. (Original) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a first plurality of independent source follower circuits, each providing a different effect on the upper trip point level when selected, and a second plurality of independent source follower circuits, each providing a different effect on the lower trip point level when selected, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one circuit in the first plurality of circuits and one circuit in the second plurality of circuits.

21. (Original) The circuit of claim 20 wherein the circuits in the first plurality of source follower circuits comprise n-channel metal oxide semiconductor field-effect transistors, and the

source follower circuits in the second plurality of circuits comprise p-channel metal oxide semiconductor field-effect transistors.

22. (Original) The circuit of claim 21 wherein:

the transistors in each circuit in the first plurality of source follower circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the first plurality of source follower circuits; and

the transistors in each circuit in the second plurality of source follower circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the second plurality of source follower circuits.

23. (Original) The circuit of claim 20 wherein the one or more control signals are programmable settings.

24. (Original) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a plurality of independent source follower circuits each providing, when selected, a different effect on one of the upper trip point level and the lower trip point level, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one source follower circuit in the plurality of source follower circuits.

25. (Amended) A method of providing an adjustable hysteresis characteristic in a Schmitt trigger circuit comprising:

providing one or more control signals to the Schmitt trigger circuit; and

in response to the one or more control signals, selecting one of a first plurality of independent parallel source follower circuits to provide a first desired signal path in the Schmitt trigger circuit.

26. (Amended) The method of claim 25 further comprising:

in response to the one or more control signals, selecting one of a second plurality of independent parallel source follower circuits to provide a second desired signal path in the Schmitt trigger circuit.

27. (Original) The method of claim 25 comprising providing the one or more control signals based on the voltage level of a power supply signal in the Schmitt trigger circuit.

28. (Original) The method of claim 25 comprising programmably providing the one or more control signals .